In the Claims

1. (currently amended) A semiconductor device where during fabrication the semiconductor device comprises:

a primary layer having a critical dimension specification;

a lower layer over the primary layer, the lower layer subsequently hard mask trimmed to satisfy the critical dimension specification of the primary layer; ~~and,~~

an upper layer over the lower layer, the upper layer having a high-etching selectivity as compared to the lower layer, the upper layer substantially preventing thickness loss of the lower layer during hard mask trimming, ~~wherein~~ the lower layer and the upper layer have a substantially identical width after etching, resulting from the lower layer and the upper layer being ~~are~~ initially hard mask etched together as a single hard mask layer prior to hard mask trimming of the lower layer; and,

an etching-stop layer between the lower layer and the primary layer for when hard mask etching of both the lower layer and the upper layer together as the single hard mask layer occurs.

2. (cancelled)

3. (original) The semiconductor device of claim 1, wherein the primary layer comprises one of a silicon layer and a polysilicon layer.

4. (original) The semiconductor device of claim 1, wherein the lower layer comprises a dielectric film.

5. (original) The semiconductor device of claim 1, wherein the upper layer comprises a dielectric film.

6. (original) The semiconductor device of claim 1, wherein the lower layer is selected from a group essentially consisting of: Si3N4, SiON, and SiO2.

7. (original) The semiconductor device of claim 1, wherein the upper layer is selected from a group essentially consisting of: polysilicon, Si3N4, SiON, and SiO2.

8. (withdrawn) A method for forming a semiconductor device comprising:

patterning a photoresist layer of a semiconductor wafer also having an upper layer under the photoresist layer and over a lower layer, and a primary layer under the lower layer, the primary layer having a critical dimension specification, the upper layer having a high-etching selectivity as compared to the lower layer;

hard mask etching the lower layer and the upper layer;

hard mask trimming at least the lower layer, the lower layer hard mask trimmed to satisfy the critical dimension specification of the primary layer, the upper layer substantially preventing thickness loss of the lower layer during hard mask trimming; and,

removing the upper layer.

9. (withdrawn) The method of claim 8, further comprising removing the photoresist layer after hard mask etching and before hard mask trimming.

10. (withdrawn) The method of claim 8, further comprising etching the primary layer for shallow trench isolation.

11. (withdrawn) The method of claim 8, further comprising:

etching the primary layer for gate formation; and,

removing the lower layer.

12. (withdrawn) The method of claim 8, the semiconductor wafer also having a thin oxide layer between the lower layer and the primary layer.

13. (withdrawn) The method of claim 8, wherein the primary layer comprises one of a silicon layer and a polysilicon layer.

14. (withdrawn) The method of claim 8, wherein each of the lower layer and the upper layer comprises a dielectric film.

15. (withdrawn) The method of claim 8, wherein the lower layer is selected from a group essentially consisting of: Si3N4, SiON, and SiO2.

16. (withdrawn) The method of claim 8, wherein the upper layer is selected from a group essentially consisting of: polysilicon, Si3N4, SiON, and SiO2.

17. (currently amended) A semiconductor device formed at least in part by a method comprising:

patterning a photoresist layer of a semiconductor wafer also having an upper layer under the photoresist layer and over a lower layer, and a primary layer under the lower layer, the primary layer having a critical dimension specification, the upper layer having a high-etching selectivity as compared to the lower layer;

hard mask etching the lower layer and the upper layer together as a single hard mask layer down to an etching-stop layer between the lower layer and the primary layer, such that the lower layer and the upper layer have a substantially identical width after etching;

removing the photoresist layer;

hard mask trimming at least the lower layer, the lower layer hard mask trimmed to satisfy the critical dimension specification of the primary layer, the upper layer substantially preventing thickness loss of the lower layer during hard mask trimming;

removing the upper layer; and,

performing one or more actions selected from the group essentially consisting of:

etching the primary layer for shallow trench isolation; and,

etching the primary layer for gate formation and removing the lower layer.

18. (cancelled)

19. (original) The semiconductor device of claim 17, wherein each of the lower layer and the upper layer comprises a dielectric film.

20. (original) The semiconductor device of claim 17, wherein each of the lower layer and the upper layer is selected from a group essentially consisting of: Si3N4, SiON, and SiO2.